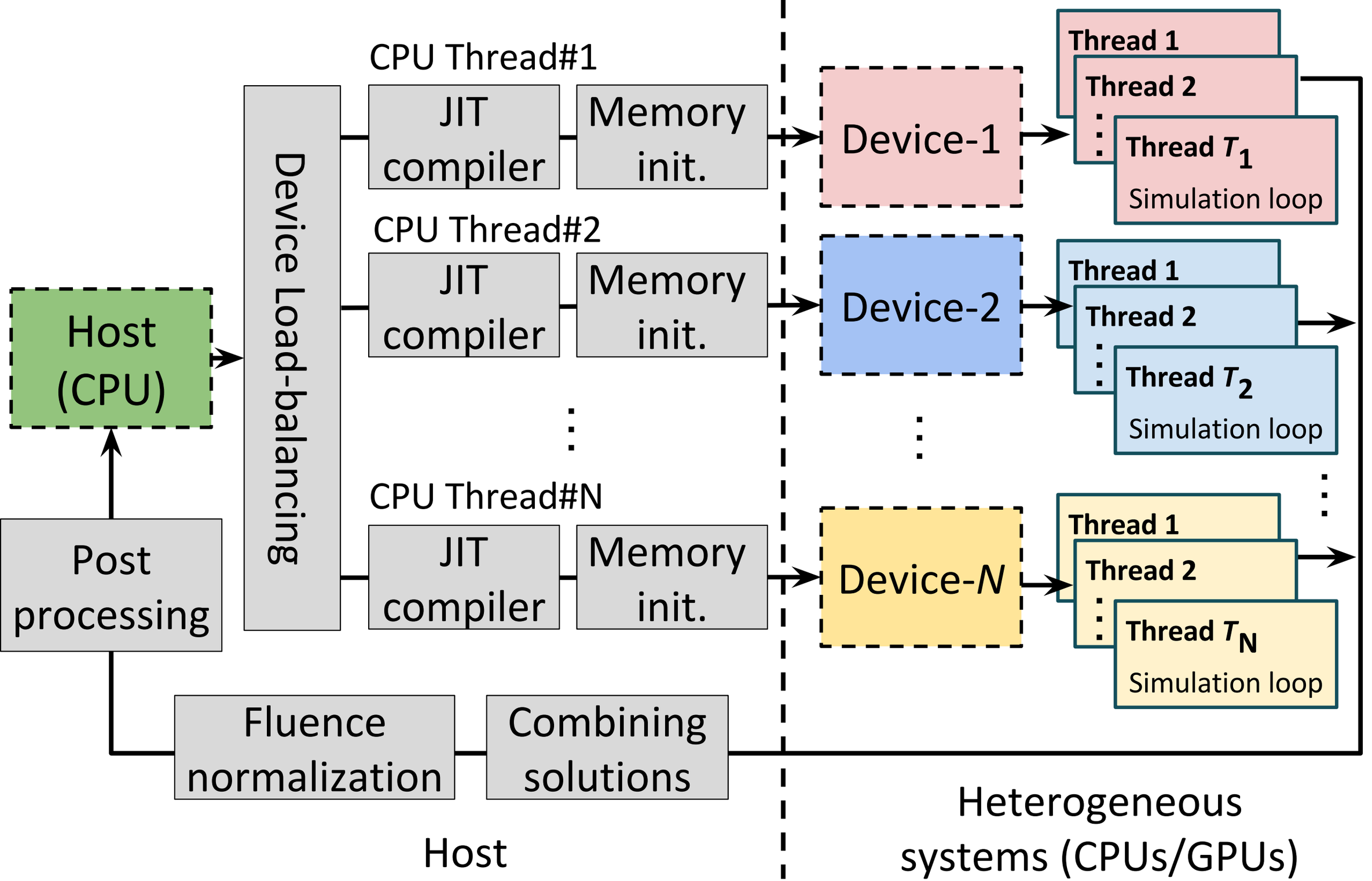
CPU Thread#1
JIT compiler
Memory init.
CPU Thread#2
JIT compiler
Memory init.
CPU Thread#N
JIT compiler
Memory init.
Device Load-balancing
Host (CPU)
Post processing
Fluence normalization
Combining solutions
Device-1
Device-2
Device-N
Thread 1
Thread 2
Thread T_1
Simulation loop
Thread 1
Thread 2
Thread T_2
Simulation loop
Thread 1
Thread 2
Thread T_N
Simulation loop
Host
Heterogeneous systems (CPUs/GPUs)